## REMARKS

In response to the Office Action dated February 10, 2006, Applicants respectfully request reconsideration based on the above claim amendments and the following remarks. Applicants respectfully submit that the claims as presented are in condition for allowance.

Claims 1-20 are pending in the present Application. Claims 1, 3, 8, 16 and 20 are amended, leaving Claims 1-20 for consideration upon entry of the present amendments and following remarks.

Support for the claim amendments is at least found in the specification, the figures, and the claims as originally filed. More particularly, support for amended Claim 1 is at least found Figure 1 and the specification at page 5, lines 20-24 and page 7, line 21 through page 9, line 4. Support for Claims 3, 8 and 16 is at least found in the specification at page 6, lines 1-4. Claim 20 is amended to better clarify the invention and support for the amendment is at least found in the specification at page 5, lines 6-8.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

***Claim Rejections – 35 USC §112***

The Examiner rejects Claims 3, 8 and 16 under 35 U.S.C. 112 as being rendered indefinite by the phrase "substantially" because the applicant discloses the same SRAM-compatible structure of the memory banks and parity bank. Reference is made to Figure 1, characters 10_i and 12 and page 6, lines 1-50 in the specification.

In response, Applicants amend Claims 3, 8 and 16 to include "a substantially same *capacity and* structure" to better define the claimed invention. Reconsideration and withdrawal of the relevant claim rejections are respectfully requested.

***Claim Rejections Under 35 U.S.C. §102***

Claims 1-20, are rejected under 35 U.S.C. §102(e) as being anticipated by Takahashi et al., U.S. Patent Publication No. 2003/0086306 (hereinafter "Takahashi"). Applicants respectfully traverse.



PAGE 9/14 * RCVD AT 5/5/2006 9:00:52 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):04-06

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Firstly, amended Claim 1 recites, *inter alia*, "a refresher timer generating a refresh request signal periodically to activate the refresh operation for both the memory banks and the parity bank." Applicants find no disclosure in Takahashi for any feature teaching a refresher timer of the claimed invention. Therefore, Takahashi does not disclose a refresher timer generating a refresh request signal periodically to activate the refresh operation for both the memory banks and the parity bank of amended Claim 1.

Regarding Claims 1 and 20, secondly, in the Office Action at Page 2, the Examiner alleges that Takahashi discloses in section [0023] "[a]n SRAM-compatible memory including a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the DRAM cells interfacing with an external system which does not provide a separate timing period for performing a refresh operation for the DRAM cells" of Claims 1 and 20. Applicants respectfully disagree.

In a non-limiting embodiment of the present invention, the internal system comprises *DRAM cells* which require regular refreshing, as recited in Claim 1. That is, the external interface is directed to SRAM compatible memory and the internal system specifically includes DRAM cells with refreshing. Takahashi discloses a sense amplifier 130 is a sense amplifier for use in the conventional SRAM. (Section [0023].) That is, the internal system of Takahashi includes the SRAM as specifically disclosed in Section [0023].

Applicants find no disclosure in Takahashi regarding anything resembling a DRAM internal system, let alone any circuit having the capacity to or in fact functioning to "refresh" as claimed, and no further explanation as to where such citation may be found is provided in the rejection details of the Office Action. Therefore, Takahashi fails to disclose a SRAM-compatible memory *including a plurality of memory banks each having a plurality of DRAM cells* arranged in a matrix form defined by rows and columns, the *DRAM cells interfacing with an external system* which does not provide a separate timing period for performing *a refresh operation for the DRAM cells* of Claims 1 and 20.



PAGE 10/14 * RCVD AT 5/5/2006 9:00:52 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):04-06

Thirdly, it is stated in the Office Action at Page 3 that Takahashi discloses the memory banks for receiving and storing input data externally provided, the memory banks generating bank information signals each indicating whether a corresponding memory bank is subjected to an invalid read-access at Section [0010], lines 6-20. Applicants respectfully disagree.

Takahashi discloses "a sense amplifier for *reading the main data* stored in the main memory, a decoder circuit that generates correction data for correcting errors generated in the main data on the basis of *the main data read from the sub-memory* and a data correction circuit that corrects the error contained in *the main data read* from the main memory corresponding to the correction data." (Section [0010], lines 6-13.) That is, there may be an error in the data, but the data itself is read without any indication of the validity of the read-access.

Applicants are unclear what feature of the sense amplifier, main memory, decoder circuit, sub-memory and data correction circuit is being considered "the memory bank" of the claimed invention. For purposes of this response, Applicants consider the main memory and the sub-memory as disclosing "the memory bank" of the claimed invention. If the Examiner disagrees with this understanding, Applicants request the Examiner to provide further explanation.

Takahashi merely discloses the functions and positions of the sense amplifier, decoder circuit and the correction circuit and provides no functioning of the main memory and the sub-memory whatsoever, let alone the main memory and the sub-memory generating any type of a signal to indicate the validity of the read-access condition of these features. Applicants find no disclosure in Takahashi regarding anything resembling the sense amplifier, main memory, decoder circuit, sub-memory and data correction circuit having the capacity to or in fact generating any type of a signal to indicate the validity of the read-access condition of these features.

To the contrary of the claimed invention, Takahashi only discloses that the main data is clearly read and that only an error in the data itself may be corrected, where the read-access condition is not considered in any way. Additionally, no further explanation as to where such citation in Takahashi may be found is provided in the rejection details of the Office Action. Therefore, Takahashi fails to disclose the *memory banks* for receiving and storing input data externally provided, the memory banks generating *bank information signals* each indicating



PAGE 11/14 * RCVD AT 5/5/2006 9:00:52 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):04-06

whether a corresponding memory bank is subjected to *an invalid read-access* of Claims 1 and 20.

Fourthly, it is further stated in the Office Action at Page 3 that Takahashi discloses a parity bank for storing the input parity and generating a parity information signal indicating whether the parity bank is subjected to the invalid read-access in Fig. 1, reference character 120. Applicants respectfully disagree.

Regarding Fig. 1, Takahashi discloses a memory unit 100 including a main memory array 110 storing data and sub-memory arrays 120 storing error correction data. (Section [0021].) The sub-memory contains error code sub-data *corresponding to the main data.* (Section [0010], lines 3-6.) That is, the error code sub-data has nothing to do with anything of a condition or functioning of anything resembling a memory bank, but only relates to the data itself.

As discussed above, Takahashi fails to disclose the sub-memory having any functioning whatsoever, let alone generating an information signal indicating whether the sub-memory is subjected to an invalid read-access as claimed. The error correction code EC is stored in sub-memory 120. (Section [0022], lines 3-5 and Section [0026].) To the contrary of the claimed invention, Takahashi only discloses that the sub-memory saves the "error correction code," is itself only read and that only an error in the data itself may be corrected, where the read-access condition is not considered in any way relating to the sub-memory.

Additionally, as discussed above, Takahashi fails to disclose the sub-memory 120 including DRAM cells and only discloses SRAM cells. Therefore, Takahashi fails to disclose a parity bank for storing the input parity and *generating a parity information signal* indicating whether the parity bank is subjected to *the invalid read-access* of Claims 1 and 20.

Finally, regarding Claims 1 and 20, it is further stated in the Office Action at Pages 3 and 4 that Takahashi discloses a data corrector receiving the bank information signals and fetched data from the memory banks and generating output data having same value as the input data by correcting data fetched from a memory bank subjected to the invalid read-access if a checked parity value is different from the preset parity value, the checked parity value being obtained using the fetched data provided from the memory banks and parity data fetched from the parity bank in Fig. 1, reference characters 250 and 300. Applicants respectfully disagree.



PAGE 12/14 * RCVD AT 5/5/2006 9:00:52 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):04-06

As discussed above, Takahashi discloses nothing of the validity of the read-access for the main memory or sub-memory (considered as the memory bank or parity bank of the claimed invention). Therefore, Takahashi necessarily does not disclose a data corrector generating output data having same value as the input data by correcting data fetched from a memory bank *subjected to the invalid read-access* if a checked parity value is different from the preset parity value of Claims 1 and 20.

Notwithstanding that Takahashi fails to consider the validity of the read-access for the main memory or sub-memory, the EDD decoder 250 and error correction circuit (ECC) 300 identify and correct error through a predetermined error correction algorithm. That is, the error detecting mechanism of Takahashi is activated even when there is not an error, contrary to the claimed invention. Therefore, Takahashi further fails to disclose a data corrector generating output data having same value as the input data by correcting data fetched from a memory bank *subjected to the invalid read-access* if a checked parity value is different from the preset parity value of Claims 1 and 20.

Regarding Claim 6, in the Office Action at Page 6, the Examiner alleges that Takahashi discloses in sections [0041] and [0042] the refresh operation is independently performed with respect to the respective memory banks, and is prevented from being simultaneously performed with respect to two or more memory banks as claimed. Applicants respectfully disagree.

Sections [0041] and [0042] describe the process of the ECC decoder 250 producing correcting signals and using the signals to *correct the data*. Correction signal COR corresponds to a bit in error correction data ED output *from the ECC decoder 250*. (Figures 1-3 and Sections [0041] and [0042].) The data is corrected, not refreshed with respect to the main memory or the sub-memory. That is, the data is being corrected in these cited sections, not "refreshed" as claimed. Therefore, Takahashi fails to disclose the *refresh operation* is independently performed *with respect to the respective memory banks* of Claim 6.

Moreover, even if Takahashi's error correction may be considered as a "refresh" operation, Applicants find no disclosure in Takahashi as to preventing the error correction from being simultaneously performed with respect to two or more of the main memory and sub-memory (considered as memory banks of the claimed invention). Therefore, Takahashi further fails to disclose the refresh operation is independently performed with respect to the respective



PAGE 13/14 * RCVD AT 5/5/2006 9:00:52 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):04-06

memory banks, and is *prevented from being simultaneously performed* with respect to *two or more memory banks* of Claim 6.

Thus, Takahashi fails to disclose all of the limitations of at least Claims 1 (as amended), 6 and 20. Accordingly, Takahashi does not anticipate Claims 1 (as amended), 6 and 20. Claims 1, 6 and 20 are not further rejected or objected and are therefore allowable. Claims 2-5 and 7-19 variously depend from Claim 1, are not further rejected or objected and are correspondingly allowable as depending upon allowable Claim 1. Reconsideration and allowance of Claims 1-20 are respectfully requested.

***Conclusion***

All of the objections and rejections are herein overcome. In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. No new matter is added by way of the present Amendments and Remarks, as support is found throughout the original filed specification, claims and drawings. Prompt issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact Applicants' attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicants hereby petition for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,

CANTOR COLBURN LLP

By: Amy Bizon-Copp

Amy Bizon-Copp
Reg. No. 53,993
CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002
Telephone (860) 286-2929
Facsimile (860) 286-0115

Date: May 5, 2006



PAGE 14/14 * RCVD AT 5/5/2006 9:00:52 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):04-06